REMARKS

Applicant thanks the Examiner for the careful consideration given to this application. Reconsideration is now respectfully requested in view of the following remarks.

Claims 1-62 are pending in this application. Claims 1, 10, 19, 31, 40, 41, 47, 51, 55, 56, 57, 61 and 62 are independent claims. Claims 10-30, 41-50, 56, and 62 were previously withdrawn. Reconsideration and allowance of the present application are respectfully requested.

Allowable Subject Matter

Applicants note with appreciation the allowance of Claims 1-9 and the indication that claims 2-9, 32-39 and 52-54 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections under 35 U.S.C. § 102

Claims 31, 40, 51, 55, 57 and 61 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 7,134,005 to Henry et al. (hereinafter "Henry et al."). These rejections are respectfully traversed for at least the following reasons.

The following discussion uses Claim 31 as an example; however, the arguments are applicable to the other independent claims (40, 51, 55, 57, and 61), which, although of varying scopes, contain at least some similar features.

Claim 31 recites:

A circuit for use in a first access point comprising:

a first circuit configured to identify receipt of a first data packet;

a second circuit configured to issue a response to the first data packet; and

wherein the first access point is configured to transmit the response before the first access point has completed a packet decoding operation on the first data packet.

The Office Action, at page 2, cites Henry et al. at col. 8, line 56 to col. 9, line 3 and at col. 32, lines 14-28 as disclosing all of the subject matter of the independent claims listed in this rejection.

At col. 8, line 56 to col. 9, line 3, Henry et al. states:

> In another aspect, it is a feature of the present invention to provide a method in a microprocessor for recovering from an erroneous branch to a speculative target address of a presumed branch instruction. The method includes providing a speculative target address in response to an instruction cache fetch address, producing an instruction cache line in response to the instruction cache fetch address, and decoding an instruction from the instruction cache line subsequent to the providing the speculative target address. The decoding is performed for a first time by the microprocessor for the instruction. The method also includes branching to the speculative target address prior to the decoding, and branching to a correct target address of the instruction subsequent to the branching to the speculative target address in response to the decoding.

Henry et al. at col. 8, line 56 to col. 9, line 3. At col. 32, lines 14-28, Henry et al. states:

> Referring now to FIG. 14, a flowchart illustrating operation of the branch prediction apparatus 400 of FIG. 4 to selectively override speculative branch predictions with non-speculative branch predictions thereby improving the branch prediction accuracy of the present invention is shown. After an instruction is received from the instruction buffer 342, the instruction decode logic 436 of FIG. 4 decodes the instruction and the non-speculative target address calculator 416, non-speculative call/return stack 414, and non-speculative branch direction predictor 412 of FIG. 4 generate non-speculative branch predictions in response to the instruction decode information 492 of FIG. 4, in step 1402. The instruction decode logic 436 generates a type of the instruction provided in the instruction decode information 492, in step 1402.

Henry et al. at col. 32, lines 14-28. Applicants respectfully submit that there are numerous differences between what is found in Claim 1 and what is disclosed in Henry et al.

As an initial observation, it is apparent that Henry et al. is not directed to any "circuit" whatsoever and does not treat any "access point." As discussed, e.g., at col. 1, lines 35-37, Henry et al. is directed to "the field of branch prediction in microprocessors, and more particularly to branch target address caching." Henry et al. at col. 1, lines 35-37. This is an altogether different field of endeavor from the claimed subject matter. It addresses an altogether different problem in an altogether different way. Hence, one of ordinary skill in the art would not have looked to Henry et al. to solve any problem solved by the claimed subject matter; consequently, Applicant submits that it is not proper to reject the claims based on Henry et al.

Now, addressing the specific elements in the body of Claim 31 (and again, the other rejected independent claims, although of different scopes, contain one or more similar features), Claim 31 includes, "a first circuit configured to identify receipt of a first data packet." Applicant has found no disclosure, in either the cited passages or anywhere else in Henry et al., of any such circuit or of "identify[ing] receipt of a first data packet." In fact, Henry et al. is directed to methods for use within a microprocessor and does not teach any circuits, *per se*, other than circuits within the microprocessor in which the methods are to be implemented.

To delve deeper into this difference between Henry et al. and the claimed subject matter, each of the independent claims refers to "identify[ing] receipt of a first data packet." However, a careful consideration of Henry et al., noting the cited portions, as well as Fig. 4 (described at col. 12, lines 59-60 as "a speculative branch prediction apparatus 400 of the processor 300") and its accompanying discussion at cols. 12-19, reveals that in Henry et al., instructions are "fetched." Therefore, the apparatus, e.g., of Fig. 4 of Henry et al., does not need to "identify receipt of a first data packet" because it fetches instructions and thus is aware of the presence of the instructions.

Applicant further notes that the Office Action fails to identify any "first circuit" that is "configured to indentify receipt of a first data packet."

Consequently, the Office Action fails to establish that Henry et al. discloses "a first circuit configured to identify receipt of a first data packet."

Moving to the next element of Claim 31, Claim 31 further includes, "a second circuit configured to issue a response to the first data packet." Again, Applicant has found no disclosure, in either the cited passages or anywhere else in Henry et al., of any such circuit or of "issu[ing] a response to the first data packet." Again, Henry et al. does not address acting upon any received data packets; rather, Henry et al. addresses branch prediction in microprocessors. Furthermore, the Office Action fails to identify any such "second circuit" in Henry et al. Consequently, the Office Action also fails to establish that Henry et al. discloses the claimed "second circuit."

Finally, Claim 31 recites, "wherein the first access point is configured to transmit the response before the first access point has completed a packet decoding operation on the first data packet." Applicant notes, again, that Henry et al. fails to address or even mention an "access point" and is unrelated to "access point" technology. There is also no mention of "transmitting the response [by the first access point]." Furthermore, the Office Action fails to identify how Henry et al. allegedly discloses such features.

As noted above, the above reasoning applies to Claims 40, 51, 55, 57, and 61, as well as to Claim 31. However, there are further features found in at least some of these claims, which Henry et al. also fails to disclose.

Claim 41 includes the recitation of "a terminal configured to communicate with at least a second access point." Nowhere in the cited portions of Henry et al. has Applicant found any disclosure of such a "terminal" or mention of "at least a second access point," nor has the Office Action identified any such specific disclosures in Henry et al.

Claim 51 is directed to an apparatus, including "means for identifying receipt of a first data packet;" "means for issuing a response to the first data packet;" and "means for transmitting a response before decoding the first data packet." The Office Action fails to identify any disclosures of Henry et al. corresponding to any of these elements.

Claim 55, of differing scope from but similar to Claim 51, also includes "means for communicating with at least a second access point." Claim 61 similarly includes, "communicating with at least a second access point." Again, the Office Action fails to identify any disclosure of Henry et al. that corresponds to such elements.

For at least these reasons, Applicant respectfully submits that the Office Action fails to present a *prima facie* case for the anticipation of any of Claims 31, 40, 51, 55, 57, and 61 by Henry et al.

Therefore, Applicant respectfully requests that this rejection under 35 U.S.C. § 102 be withdrawn.

Disclaimer

Applicant may not have presented all possible arguments or have refuted the characterizations of either the claims or the prior art as found in the Office Action. However, the lack of such arguments or refutations is not intended to act as a waiver of such arguments or as concurrence with such characterizations.

CONCLUSION

In view of the above, consideration and allowance are respectfully solicited.

In the event the Examiner believes an interview might serve in any way to advance the prosecution of this application, the undersigned is available at the telephone number noted below.

The Office is authorized to charge any necessary fees to Deposit Account No. 22-0185.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 22-0185, under Order No. 27592-00275-US3 from which the undersigned is authorized to draw.

Dated: December 7, 2010

Respectfully submitted,

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